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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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  ```
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  ```

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  ```
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  ```

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  ```
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  ```

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  ```
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  ```

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  ```

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  ```
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```
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1 SAFE-OPS: An approach to embedded software security

Joseph Zambreno, Alok Choudhary, Rahul Simha, Bhagi Narahari, Nasir Memon

February 2005 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 4 Issue 1

Publisher: ACM Press

Full text available: pdf(556.27 KB) Additional Information: full citation, abstract, references, index terms

The new-found ubiquity of embedded processors in consumer and industrial applications brings with it an intensified focus on security, as a strong level of trust in the system software is crucial to their widespread deployment. The growing area of *software protection* attempts to address the key steps used by hackers in attacking a software system. In this paper, we introduce a unique approach to embedded software protection that utilizes a hardware/software codesign methodology. Results d ...

Keywords: HW/SW codesign, Software protection

2 Track 13: special purpose architectures: A combined hardware and software architecture for secure computing

Jürg Platte, Edwin Naroska

May 2005 **Proceedings of the 2nd conference on Computing frontiers**

Publisher: ACM Press

Full text available: pdf(507.25 KB) Additional Information: full citation, abstract, references, index terms

Remote code execution becomes more and more important as can be seen by Grid computing or distributed computing projects like SETI@home. However, executing programs on foreign computers leads to security risks if the program contains sensitive data or algorithms. Current operating systems can protect user programs from other malicious programs running on the same host. But this does not prevent attacks from a system administrator or a malicious operating system. Further, even if the operating sy ...

Keywords: certified execution, encrypted programs, secure processors

3 Prototyping, verification, and test: Implementation of BEE: a real-time large-scale hardware emulation engine

Chen Chang, Kimmo Kuusilinna, Brian Richards, Robert W. Brodersen

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(3.65 MB) Additional Information: full citation, abstract, references, index terms

This paper describes the hardware implementation of a real-time, large-scale, multi-chip FPGA (Field Programmable Gate Array) based emulation engine with a capacity of 10 million ASIC (Application Specific Integrated Circuits) equivalent gates. Attainable system operation frequency can exceed 60 MHz, and the system throughput has been empirically verified to achieve 600 billion 16-bit additions per second. The emulator is custom designed to maximize the performance and resource utilization for a ...

Keywords: FPGA, hardware emulation, rapid-prototyping

4 Embedded applications: Encryption overhead in embedded systems and sensor network nodes: modeling and analysis

Ramnath Venugopalan, Prasanth Ganesan, Pushkin Peddabachagari, Alexander Dean, Frank Mueller, Mihail Sichitiu

October 2003 **Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems**

Publisher: ACM Press

Full text available: pdf(293.59 KB) Additional Information: full citation, abstract, references, citings, index terms

Recent research in sensor networks has raised issues of security for small embedded devices. Security concerns are motivated by the deployment of a large number of sensory devices in the field. Limitations in processing power, battery life, communication bandwidth and memory constrain the applicability of existing cryptography standards for small embedded devices. A mismatch between wide arithmetic for security (32 bit word operations) and embedded data bus widths (often only 8 or 16 bits) combi ...

Keywords: embedded systems, encryption, security, sensor networks

5 Security: Analyzing and modeling encryption overhead for sensor network nodes

Prasanth Ganesan, Ramnath Venugopalan, Pushkin Peddabachagari, Alexander Dean, Frank Mueller, Mihail Sichitiu

September 2003 **Proceedings of the 2nd ACM international conference on Wireless sensor networks and applications**

Publisher: ACM Press

Full text available: pdf(254.57 KB) Additional Information: full citation, abstract, references, index terms

Recent research in sensor networks has raised security issues for small embedded devices. Security concerns are motivated by the deployment of a large number of sensory devices in the field. Limitations in processing power, battery life, communication bandwidth and memory constrain the applicability of existing cryptography standards for small embedded devices. A mismatch between wide arithmetic for security (32 bit word operations) and embedded data bus widths (often only 8 or 16 bits) combined ...

Keywords: analysis, embedded systems, encryption overhead, model, sensor networks

6 Agreement problems: Self-stabilizing byzantine agreement

Ariel Daliot, Danny Dolev

July 2006 **Proceedings of the twenty-fifth annual ACM symposium on Principles of distributed computing PODC '06**

Publisher: ACM Press

Full text available: pdf(290.99 KB) Additional Information: full citation, abstract, references, index terms

Byzantine agreement algorithms typically assume implicit initial state consistency and synchronization among the correct nodes and then operate in coordinated rounds of information exchange to reach agreement based on the input values. The implicit initial assumptions enable correct nodes to infer about the progression of the algorithm at other nodes from their local state. This paper considers a more severe fault model than permanent Byzantine failures, one in which the system can in addition b ...

Keywords: byzantine agreement, byzantine faults, pulse synchronization, reliable broadcast, self-stabilization, transient failures

Results 1 - 6 of 6

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L1	79	713/189-194.ccls. and (data adj rate)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 09:31
L2	37	tampe$ same ((data write) adj rate)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 09:40
L3	36	713/189-194.ccls. and ((erase scrub format degauss) adj (memory ram))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 09:42
L4	66	713/189-194.ccls. and ((erase scrub format degauss overwrit$) adj (memory ram))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:02
L5	83	713/189-194.ccls. and (clock adj (rate frequency))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:35
L6	2	((erase scrub format) adj (ram memory)) and (power adj analysis)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:37
L7	0	((overwrite (over adj write)) adj (ram memory)) and (power adj analysis)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:38
L8	27	(overwrite (over adj write)) and (power adj analysis)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 14:41

EAST Search History

L9	1206	clock same (tamper tampering)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 14:41
L10	1044	(clock same (tamper tampering)) and memory	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 14:42
L11	705	(clock same (tamper tampering)) and ram	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 14:42
L12	199	((clock adj (generat$ rate)) same (tamper tampering)) and ram	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 14:43
L13	5	("5115393" \| "5467396" \| "5475855" \| "5808961" \| "6606707").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/06 15:25
L14	3	326/8.ccls. and (clock adj (rate speed))	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/06 15:25